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S/N 09/551,027 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner: Michael Trinh
Serial No.:	09/551,027	Group Art Unit: 2822
Filed:	April 17, 2000	Docket: 303.379US2
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Applicants have included the fee of $180.00 under 37 C.F.R. §§ 1.97(c) and 1.17(p). Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

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Date 6/5/2001 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 5th day of June, 2001.

Amy Moriarty
Name

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Signature